CLAIM AMENDMENTS

Claims 1-24 (CANCELED).

25(PREVIOUSLY PRESENTED). A data processing system, comprising:

a system bus;

a first bus master coupled to the system bus;

a second bus master coupled to the system bus;

a resource coupled to the system bus and useable by the first bus master and the second bus master, wherein the resource is configurable to be owned by at least one of the first bus master and the second bus master; and

additional signal steering logic which establishes a communication path between the resource and at least one of the first bus master and the second bus master, wherein the communication path is used to transfer at least one additional signal between the resource and the at least one of the first bus master and the second bus master, and wherein the communication path is determined by the resource.

26(PREVIOUSLY PRESENTED). The data processing system of claim 25, wherein the communication path is determined by a current state of the resource.

27(PREVIOUSLY PRESENTED). The data processing system of claim 26, wherein the current state of the resource comprises an operating mode of the resource.

28(CURRENTLY AMENDED). The data processing system of claim 25, wherein the communication path is determined based on a map definition defined by the resource.

29(PREVIOUSLY PRESENTED). The data processing system of claim 28, wherein the additional signal steering logic comprises map definition storage circuitry which stores the map definition.

30(PREVIOUSLY PRESENTED). The data processing system of claim 25, wherein the additional signal steering logic establishes the communication path between the resource and both the first bus master and the second bus master.

31(PREVIOUSLY PRESENTED). The data processing system of claim 25, wherein the at least one additional signal is not a part of the system bus.

32(PREVIOUSLY PRESENTED). The data processing system of claim 25, wherein the system bus operates according to a system bus protocol, and the at least one additional signal operates outside the system bus protocol.

33(PREVIOUSLY PRESENTED). The data processing system of claim 25, wherein the resource comprises at least a portion of the additional signal steering logic.

34(PREVIOUSLY PRESENTED). A method for communicating an additional signal in a data processing system having a system bus, comprising:

establishing a communication path between a resource coupled to the system bus and at least one of a plurality of bus masters coupled to the system bus, wherein the communication path is determined by the resource; and

transferring the additional signal, separate from the system bus, between the resource and the at least one of the plurality of bus masters via the communication path.

35(PREVIOUSLY PRESENTED). The method of claim 34, wherein establishing the communication path comprises:

determining a current state of the resource; and

establishing the communication path based on the current state of the resource.

36(PREVIOUSLY PRESENTED). The method of claim 34, wherein establishing the communication path comprises:

providing a map definition defined by the resource; and

establishing the communication path based on the map definition.

37(NEW). A data processing system, comprising:

a system bus;

a first bus master coupled to the system bus;

a second bus master coupled to the system bus; and

a resource coupled to the system bus and useable by the first bus master and the second bus master,

wherein the resource comprises:

endpoint storage circuitry comprising a plurality of endpoints,

wherein each of the plurality of endpoints is allocatable to at least one of the first bus master and the second bus master, and wherein allocatability of each of the plurality of endpoints is programmable.

38(NEW). A data processing system as in claim 37, wherein the resource further comprises:

a controller, coupled to the endpoint storage circuitry, the controller comprising:

interrupt steering registers; and

interrupt steering logic,

wherein the interrupt steering logic routes interrupts to a corresponding one of the first bus master and the second bus master based on steering information provided by the interrupt steering registers.

39(NEW). A data processing system as in claim 38, wherein the plurality of endpoints are allocated based on the interrupt steering registers.

40(NEW). A data processing system as in claim 38, wherein for each of the plurality of endpoints, the interrupt steering registers indicate allocation to one of the first bus master and the second bus master.

41(NEW). A data processing system as in claim 38, wherein the interrupt steering registers comprise an interrupt steering set register and an interrupt steering clear register.

42(NEW). The A data processing system as in claim 41, wherein the interrupt steering registers further comprise interrupt steering storage circuitry coupled to the interrupt steering set register and the interrupt steering clear register, the interrupt steering storage circuitry providing the steering information to the interrupt steering logic.

43(NEW). The A data processing system as in claim 42, wherein the interrupt steering storage circuitry comprises a plurality of set-reset latches.

44(NEW). A method for communicating an additional signal in a data processing system having a system bus, the method comprising:

providing a first bus master coupled to the system bus;
providing a second bus master coupled to the system bus;
providing a resource coupled to the system bus;
providing a programmable circuit in the resource;
establishing a communication path between the resource and at least one of the first and second bus masters,
wherein the communication path is determined by the programmable circuit in the resource, and
wherein no additional steering logic is required in the communication path between the resource and the at least one of the first and second bus masters; and
transferring an additional signal, separate from the system bus, between the resource and the at least one of the first and second bus masters via the communication path.

45(NEW). A method as in claim 44, wherein the additional signal comprises an interrupt signal.

46(NEW). A method as in claim 44, wherein the additional signal comprises a DMA signal.

47(NEW). A method as in claim 44, wherein the additional signal comprises a reset signal.

48(NEW). A method as in claim 44, wherein the additional signal comprises a power control signal.

49(NEW). A method as in claim 44, wherein the resource comprises a plurality of USB endpoints.

50(NEW). A method as in claim 44, wherein the programmable circuit in the resource comprises a set register and a clear register.

51(NEW). A method as in claim 50, wherein the programmable circuit in the resource further comprises a plurality of set/reset latches, wherein the set register provides set signals to the plurality of set/reset latches, and wherein the clear register provides reset signals to the plurality of set/reset latches.

52(NEW). A method as in claim 50, further comprising:

allowing the first bus master to program the set register during a first bus cycle of the system bus; and

allowing the second bus master to program the clear register during a second bus cycle of the system bus,

wherein the second bus cycle is subsequent to the first bus cycle.

53(NEW). A method as in claim 44, wherein the resource comprises a first plurality of endpoints allocated to the first bus master, and the resource comprises a second plurality of endpoints allocated to the second bus master.

54(NEW). A method as in claim 53, wherein the resource is unowned by the first bus master, and the resource is unowned by the second bus master.

55(NEW). A method as in claim 44, wherein the first bus master and the second bus master share control of the programmable circuit in the resource.

56(NEW). A method as in claim 44, wherein transferring of the additional signal is not aborted because the resource is unowned by the first and second bus masters.